CLAIMS

WHAT IS CLAIMED IS:

1. A modulator that modulates an information signal onto a carrier signal to produce a modulated information signal, the modulator comprising:

a generating circuit that produces a first modulating signal that corresponds to those portions of the information signal having positive values and a second modulating signal that corresponds to those portions of the information signal having negative values;

a first half modulator that modulates the carrier signal with the first modulating signal to produce a first half modulated signal;

a second half modulator that modulates the carrier signal with the second modulating signal to produce a second half modulated signal; and

a combining circuit that combines the first half modulated signal and the second half modulated signal to produce the modulated information signal.

2. The modulator according to Claim 1 wherein the generating circuit comprises a sorter that sorts the portions of the information signal having positive values and the portions of the information signal having negative values to produce the first and second modulating signals.

3. The modulator according to Claim 1 wherein the generating circuit comprises:

a first sigma-delta converter that is responsive to the portions of the information signal having positive values to produce the first modulating signal as a first sigma-delta bitstream; and

a second sigma-delta converter that is responsive to the portions of the information signal having negative values to produce the second modulating signal as a second sigma-delta bitstream.

4. The modulator according to Claim 3 further comprising:

a first current source that is enabled and disabled in response to the first sigma-delta bitstream, wherein the first half modulator modulates the carrier signal in response to the first current source to produce the first half modulated signal; and

a second current source that is enabled and disabled in response to the second sigma-delta bitstream, wherein the second half modulator modulates the carrier signal in response to the second current source to produce the second half modulated signal.

5. The modulator according to Claim 4 further comprising:

a first low pass filter that connects the first current source to the first half modulator; and

a second low pass that connects the second current source to the second half modulator.

6. The modulator according to Claim 1 further comprising:

a first current source that is enabled and disabled in response to the first modulating signal, wherein the first half modulator modulates the carrier signal in response to the first current source to produce the first half modulated signal; and

a second current source that is enabled and disabled in response to the second modulating signal, wherein the second half modulator modulates the carrier signal in response to the second current source to produce the second half modulated signal.

7. The modulator according to Claim 6 further comprising:

a first low pass filter that connects the first current source to the first half modulator; and

a second low pass filter that connects the second current source to the second half modulator.

8. The modulator according to Claim 1:

wherein the first half modulator comprises a first current mirror circuit that is responsive to the first modulating signal to produce a current scaled replica of the first modulating signal; and

wherein the second half modulator comprises a second current mirror circuit that is responsive to the second modulating signal to produce a current scaled replica of the second modulating signal.

9. The modulator according to Claim 8:

wherein the first half modulator further comprises a first switching circuit that switches the current scaled replica of the first modulating signal at a rate that is based upon the carrier signal; and

wherein the second half modulator further comprises a second switching circuit that switches the current scaled replica of the second modulating signal at a rate that is based upon the carrier signal.

10. The modulator according to Claim 1 wherein the combining circuit comprises a node that directly couples the first half modulated signal and the second half modulated signal to produce the modulated information signal.

11. The modulator according to Claim 1 wherein the information signal is a ternary valued information signal comprising a stream of ternary digits each having notational values of +1, 0 and –1, and wherein the generating circuit produces the first modulating signal that comprises first logic levels that correspond to the ternary digits having +1 notational values and second logic levels, and the second modulating signal that comprises first logic levels that correspond to the ternary digits having -1 notational values and second logic levels.

12. The modulator according to Claim 11 further comprising:

a first current source that is enabled by the first logic levels of the first modulating signal and is disabled by the second logic levels of the first modulating signal, wherein the first half modulator modulates the radio frequency carrier signal in response to the first current source to produce the first half modulated signal; and

a second current source that is enabled by the first logic levels of the second modulating signal and is disabled by the second logic levels of the second modulating signal, wherein the second half modulator modulates the radio frequency carrier signal in response to the second current source to produce the second half modulated signal.

13. The modulator according to Claim 12 further comprising:

a first low pass filter that connects the first current source to the first half modulator; and

a second low pass filter that connects the second current source to the second half modulator.

14. A quadrature modulator that modulates an information signal onto a carrier signal to produce a modulated information signal, the quadrature modulator comprising:

a generating circuit that produces in-phase (I) samples and quadrature (Q) samples of the information signal;

a converter that converts the I samples of the information signal into a continuous I waveform and a continuous complementary-I waveform, and that also converts the Q samples of the information signal into a continuous Q waveform and a continuous complementary-Q waveform;

at least one current mirror that is responsive to the converter to produce proportional currents that are proportional to the continuous I waveform, the continuous complementary-I waveform, the continuous Q waveform and the continuous complementary-Q waveform; and

a switching circuit that alternatingly switches the proportional currents to first and second output terminals under control of switching signals at a frequency of the carrier signal to produce the modulated information signal at the first and second output terminals.

15. The quadrature modulator according to Claim 14:

wherein the converter converts the I samples into a continuous I waveform and a continuous complementary-I waveform such that a difference between the continuous I waveform and the continuous complementary-I waveform represents a real part of the information signal; and

wherein the converter converts the Q samples into a continuous Q waveform and a continuous complementary-Q waveform such that a difference between the continuous Q waveform and the continuous complementary-Q waveform represents an imaginary part of the information signal.

16. The quadrature modulator according to Claim 14:

wherein the converter converts the I samples into a continuous I waveform and a continuous complementary-I waveform such that the continuous I waveform

represents positive portions of a real part of the information signal and the continuous complementary-I waveform represents negative portions of the real part of the information signal; and

wherein the converter converts the Q samples into a continuous Q waveform and a continuous complementary-Q waveform such that the continuous Q waveform represents positive portions of an imaginary part of the information signal and the continuous complementary-Q waveform represents negative portions of the imaginary part of the information signal.

17. The quadrature modulator according to Claim 14 wherein the generating circuit comprises at least one sigma-delta converter.

18. A quadrature modulator comprising:

a quadrature splitter; and

a pair of Gilbert Multiplier Cells coupled to the quadrature splitter, each of which is biased in Class-B.

19. The quadrature modulator according to Claim 18 wherein each of the Gilbert Multiplier Cells comprises:

a pair of cross-coupled emitter-coupled transistor pairs; and

at least one current mirror circuit that is coupled to at least one of the emitter-coupled transistor pairs.

20. The quadrature modulator according to Claim 18 further comprising:

at least one current source that selectively applies current to the pair of Gilbert Multiplier Cells to thereby bias the pair of Gilbert Multiplier Cells in Class-B.

21. The quadrature modulator according to Claim 19 further comprising:

at least one current source that selectively applies current to the at least one current mirror circuit to thereby bias the pair of Gilbert Multiplier Cells in Class-B.

22. A Gilbert Multiplier Cell comprising:

a pair of cross-coupled emitter-coupled transistor pairs; and

a driver circuit that is coupled to at least one of the emitter-coupled transistor pairs and that is biased in Class-B.

23. The Gilbert Multiplier Cell according to Claim 22 wherein the driver circuit comprises at least one current mirror circuit that is coupled to at least one of the emitter-coupled transistor pairs.

24. The Gilbert Multiplier Cell according to Claim 22 wherein the driver circuit comprises at least one current source that selectively applies current to at least one of the emitter-coupled transistor pairs.

25. The Gilbert Multiplier Cell according to Claim 23 wherein the driver circuit further comprises:

at least one current source that selectively applies current to the at least one current mirror circuit.

26. A wireless terminal comprising:

a processor that processes input signals; and

a quadrature modulator that is responsive to the processor, the quadrature modulator comprising a quadrature splitter, and a pair of Gilbert Multiplier Cells coupled to the quadrature splitter, each of which is biased in Class-B.

27. The wireless terminal according to Claim 26 wherein each of the Gilbert Multiplier Cells comprises:

a pair of cross-coupled emitter-coupled transistor pairs; and

at least one current mirror circuit that is coupled to at least one of the emitter-coupled transistor pairs.

28. The wireless terminal according to Claim 26 further comprising:

at least one current source that selectively applies current to the pair of Gilbert Multiplier Cells to thereby bias the pair of Gilbert Multiplier Cells in Class-B.

29. The wireless terminal according to Claim 27 further comprising:

at least one current source that selectively applies current to the at least one current mirror circuit to thereby bias the pair of Gilbert Multiplier Cells in Class-B.

30. A method of modulating an information signal onto a carrier signal to produce a modulated information signal, the method comprising:

producing a first modulating signal that corresponds to those portions of the information signal having positive values and a second modulating signal that corresponds to those portions of the information signal having negative values;

modulating the carrier signal with the first modulating signal to produce a first half modulated signal;

modulating the carrier signal with the second modulating signal to produce a second half modulated signal; and

combining the first half modulated signal and the second half modulated signal to produce the modulated information signal.

31. The method according to Claim 30 wherein producing a first modulating signal that corresponds to those portions of the information signal having positive values and a second modulating signal that corresponds to those portions of the information signal having negative values comprises sorting the portions of the information signal having positive values and the portions of the information signal having negative values to produce the first and second modulating signals.

32. The method according to Claim 30 wherein producing a first modulating signal that corresponds to those portions of the information signal having positive values and a second modulating signal that corresponds to those portions of the information signal having negative values comprises:

sigma-delta converting the portions of the information signal having positive values to produce the first modulating signal as a first sigma-delta bitstream; and

sigma-delta converting the portions of the information signal having negative values to produce the second modulating signal as a second sigma-delta bitstream.

33. The method according to Claim 32 further comprising:

enabling and disabling a first current source in response to the first sigma-delta bitstream; and

enabling and disabling a second current source in response to the second sigma-delta bitstream.

34. The method according to Claim 33 further comprising:

low pass filtering the first current source; and

low pass filtering the second current source.

35. The method according to Claim 30 further comprising:

enabling and disabling a first current source in response to the first modulating signal; and

enabling and disabling a second current source in response to the second modulating signal.

36. The method according to Claim 35 further comprising:

low pass filtering the first current source; and

low pass filtering the second current source.

37. The method according to Claim 30:

wherein modulating the carrier signal with the first modulating signal to produce a first half modulated signal comprises producing a current scaled replica of the first modulating signal; and

wherein modulating the carrier signal with the second modulating signal to produce a second half modulated signal comprises producing a current scaled replica of the second modulating signal.

38. The method according to Claim 37:

wherein modulating the carrier signal with the first modulating signal to produce a first half modulated signal comprises switching the current scaled replica of the first modulating signal at a rate that is based upon the carrier signal; and

wherein modulating the carrier signal with the second modulating signal to produce a second half modulated signal comprises switching the current scaled replica of the second modulating signal at a rate that is based upon the carrier signal.

39. The method according to Claim 30 wherein combining the first half modulated signal and the second half modulated signal to produce the modulated information signal comprises directly coupling the first half modulated signal and the second half modulated signal to produce the modulated information signal.

40. The method according to Claim 30 wherein the information signal is a ternary valued information signal comprising a stream of ternary digits each having notational values of +1, 0 and –1, and wherein producing a first modulating signal that corresponds to those portions of the information signal having positive values and a second modulating signal that corresponds to hose portions of the information signal having negative values comprises producing the first modulating signal that comprises first logic levels that correspond to the ternary digits having +1 notational values and second logic levels, and producing the second modulating signal that comprises first logic levels that correspond to the ternary digits having -1 notational values and second logic levels.

41. The method according to Claim 40 further comprising:

enabling a first current source by the first logic levels of the first modulating signal and disabling the first current source by the second logic levels of the first modulating signal; and

enabling a second current source by the first logic levels of the second modulating signal and disabling the second current source by the second logic levels of the second modulating signal.

42. The method according to Claim 41 further comprising:

low pass filtering the first current source; and

low pass filtering the second current source.

43. A quadrature modulating method that modulates an information signal onto a carrier signal to produce a modulated information signal, the quadrature modulating method comprising:

producing in-phase (I) samples and quadrature (Q) samples of the information signal;

converting the I samples of the information signal into a continuous I waveform and a continuous complementary-I waveform, and converting the Q samples of the information signal into a continuous Q waveform and a continuous complementary-Q waveform;

producing proportional currents that are proportional to the continuous I waveform, the continuous complementary-I waveform, the continuous Q waveform and the continuous complementary-Q waveform; and

alternatingly switching the proportional currents to first and second output terminals under control of switching signals at a frequency of the carrier signal to produce the modulated information signal at the first and second output terminals.

44. The method according to Claim 43 wherein converting the I samples of the information signal into a continuous I waveform and a continuous complementary-I waveform, and converting the Q samples of the information signal into a continuous Q waveform and a continuous complementary-Q waveform comprises:

converting the I samples into a continuous I waveform and a continuous complementary-I waveform such that a difference between the continuous I waveform and the continuous complementary-I waveform represents a real part of the information signal; and

converting the Q samples into a continuous Q waveform and a continuous complementary-Q waveform such that a difference between the continuous Q waveform and the continuous complementary-Q waveform represents an imaginary part of the information signal.

45. The method according to Claim 43 wherein converting the I samples of the information signal into a continuous I waveform and a continuous complementary-I waveform, and converting the Q samples of the information signal into a continuous Q waveform and a continuous complementary-Q waveform comprises:

converting the I samples into a continuous I waveform and a continuous complementary-I waveform such that the continuous I waveform represents positive portions of a real part of the information signal and the continuous complementary-I waveform represents negative portions of the real part of the information signal; and

converting the Q samples into a continuous Q waveform and a continuous complementary-Q waveform such that the continuous Q waveform represents positive portions of an imaginary part of the information signal and the continuous complementary-Q waveform represents negative portions of the imaginary part of the information signal.

46. The method according to Claim 43 wherein producing proportional currents that are proportional to the continuous I waveform, the continuous complementary-I waveform, the continuous Q waveform and the continuous complementary-Q waveform comprises sigma-delta converting the I samples and the Q samples of the information signal.

47. A quadrature modulation method comprising:

generating in-phase and quadrature carrier signals;

biasing a pair of Gilbert Multiplier Cells in Class-B; and

applying the in-phase and quadrature carrier signals and in-phase and quadrature information signals to the pair of Gilbert Multiplier Cells that are biased in Class-B.

48. The quadrature modulation method according to Claim 47 wherein applying the in-phase and quadrature carrier signals and in-phase and quadrature information signals to the pair of Gilbert Multiplier Cells that are biased in Class-B comprises:

mirroring the in-phase and quadrature information signals as scaled currents in the Gilbert Multiplier Cells that are biased in Class-B.

49. A method of operating Gilbert Multiplier Cell comprising:

biasing the Gilbert Multiplier Cell in Class-B.

50. The method according to Claim 49 wherein biasing the Gilbert Multiplier Cell in Class-B comprises:

mirroring a current in the Gilbert Multiplier Cell.